Abstract of the Disclosure

A simultaneous bidirectional port coupled to a bus includes a synchronization circuit that synchronizes the port with another simultaneous data port coupled to the same bus. The synchronization circuit includes an output driver having an imbalanced output impedance, and includes a receiver with input hysteresis. The input hysteresis of the receiver is not satisfied unless both drivers with imbalanced output impedance coupled to the bus assert an output signal. Each driver asserts a signal on the bus when initialization of the corresponding simultaneous bidirectional port is complete. When both simultaneous bidirectional ports are initialized, the hysteresis of the receivers is satisfied, and each port is notified that both have been initialized.